IT IS CLAIMED:

1. A method of determining the quality of a non-volatile memory having a plurality of storage elements, comprising:

programming a first population of said storage elements to establish a distribution of threshold values corresponding to a first set of bias conditions; and

subsequently determining the shift in the distribution of threshold values for the first population of storage elements in response to a second set of bias conditions.

2. The method of claim 1, wherein said first population corresponds to a physical structure of said memory.

3. The method of claim 2, wherein said physical structure is a unit of erase.

4. The method of claim 1, wherein each of said storage elements has a first source-drain region and a second source-drain region and wherein the first set of bias conditions and the second set of bias conditions use differing voltage levels at the source drain regions.

5. The method of claim 4, wherein said non-volatile memory has a NAND architecture and the voltage level on a source-drain region of a selected storage element is determined by the gate voltage level on the unselected storage elements in the NAND string of the selected storage element.

6. The method of claim 4, wherein said non-volatile memory has a NAND architecture and the voltage level on a source-drain region of a selected storage element is determined by the bit-line voltage level in the NAND string of the selected storage element.

7. The method of claim 1, wherein said determining the shift in the distribution comprises determining whether the distribution has developed a tail in response to the second set of bias conditions.

8. The method of claim 1, wherein said determining the shift in the distribution comprises determining whether the shift has exceeded a predetermined criterion.

9. The method of claim 8, further comprising:

subjecting said first population to a plurality of program-erase cycles prior to said programming.

10. The method of claim 8, wherein said determining the shift in the distribution comprises determining whether the threshold value of one or more elements of the first population has exceeded a predetermined value in response to the second set of bias conditions

11. The method of claim 8, wherein said predetermined criterion is based on settable parameter stored in said memory.

12. The method of claim 1, further comprising:

programming a second population of said storage elements to establish a distribution of threshold values corresponding to the first set of bias conditions;

subsequently determining the shift in the distribution of threshold values for the second population of storage elements in response to the second set of bias conditions; and

comparing the shift in distributions for the first population with the shift in distributions for the second population.

13. The method of claim 1, wherein said method is performed as part of an initial test of said memory.

14. The method of claim 1, wherein said method is performed subsequent to the operation of said memory.

15. The method of claim 14, wherein said method is performed in response to an error correction code (ECC) response.

16. The method of claim 14, wherein said method is performed in response to the number of operations performed.

17. The method of claim 14, wherein said memory further comprises a controller and said determining is performed by the controller.

18. The method of claim 1, wherein said first population is selected at random.

19. The method of claim 1, further comprising:

logically remapping the first population in response to said determining.

20. A method of determining defective storage elements of a non-volatile memory comprising a plurality of such elements, wherein the data state of said elements is a function of their current-voltage characteristics, the method comprising:

programming a first of said storage elements to a state determined by a first current level through the storage element in response to the application of a first set of bias conditions;

applying a second set of bias conditions differing from the first set of bias conditions to the first storage element;

determining a parameter indicative of the current level through the first storage element in response to applying the second set of bias conditions; and

determining whether the first storage element is defective based upon the value of said parameter.

21. The method of claim 20, wherein said second set of bias conditions includes a control gate voltage lower than the control gate voltage in the first set of bias conditions and said determining whether the first storage element is defective comprises:

determining whether the current level through the first storage element in response to applying the second set of bias conditions is above a first current level.

22. The method of claim 21, further comprising:

subjecting the first storage element to a number of program-erase cycles prior to said programming the first storage element.

23. The method of claim 22, wherein said number of program-erase cycles is greater than a thousand.

24. The method of claim 22, wherein said method is performed as part of an initial test of said memory.

25. The method of claim 21, wherein the control gate voltage of the second set of bias conditions is approximately zero volts.

26. The method of claim 20, wherein said second set of bias conditions includes a control gate voltage higher than the control gate voltage in the first set of bias conditions and said determining whether the first storage element is defective comprises:

determining whether the current level through the first storage element in response to applying the second set of bias conditions is below a first current level.

27. The method of claim 26, wherein the control gate voltage of the second set of bias conditions is approximately twice the control gate voltage in the first set of bias conditions.

28. The method of claim 20, wherein said second set of bias conditions includes a source-drain region voltage different than a source-drain region voltage in the first set of bias conditions.

29. The method of claim 28, wherein said determining whether the first storage element is defective comprises:

determining the change in control gate voltage required to obtain the same current level through the first storage element as in response to applying the first set of bias conditions.

30. The method of claim 29, wherein said determining whether the first storage element is defective further comprises:

comparing the change in control gate voltage to a fixed criteria.

31. The method of claim 28, wherein memory has a NAND type architecture and the voltage at the source drain region of the first storage element is related to the control gate voltage of one or more of the other storage elements in the same NAND string as the first storage element.

32. The method of claim 20, wherein said method is performed as part of an initial test of said memory.

33. The method of claim 20, wherein said method is performed subsequent to the operation of said memory.

34. The method of claim 20, wherein said method is performed in response to an error correction code (ECC) response.

35. The method of claim 20, wherein said method is performed in response to the number of operations performed.

36. The method of claim 20, wherein said first storage element is selected at random.

37. The method of claim 20, further comprising:

in response to said determining whether the first storage element is defective, logically remapping the first storage element.

38. A memory system circuit, comprising:

a non-volatile semiconductor memory unit;

programming circuitry connectable to the memory unit;

bias circuitry connectable to the memory unit;

sense circuitry connectable to the memory unit; and

a control unit connectable to the programming circuitry, whereby the memory unit can be programmed to a data state, and to the bias and sense circuitry, whereby the data state of the memory unit can be verified and whereby a current flowing through a previously verified memory unit in response to an applied set of bias conditions can be determined and the previously verified memory unit is identified as defective in response to an unexpected current being so determined.

39. The memory system circuit of claim 38, wherein the memory unit includes a plurality of memory transistors connected in series, each of the memory transistors comprising a floating gate and a control gate, and wherein a given one of said memory transistors is selected to be programmed, verified, and subsequently biased to determine whether the selected transistor is defective.

40. The memory of claim 39, wherein the control gates of non-selected memory transistors have a first voltage applied when the selected memory transistor is verified and a second voltage different from the first voltage applied when the selected memory transistor is subsequently biased to determine whether the selected memory transistor is defective.